Claims

1-10 Canceled

11. (New) A method for the detection and/or correction of memory access errors in a processor system, the method comprising:

storing data which is to be secured in a memory; and

storing test data in the memory (4) in addition to the data which is to be secured, wherein in addition to the data to be secured, addresses of the data are taken into account when generating the test data.

12. (New) The method of claim 11, wherein the data to be secured is transmitted jointly with associated test data to a data receiver, and the test data is evaluated for error detection only after the data transfer.

13. (New) The method of claim 12, wherein the test data is evaluated for error detection in an error detection device that is checked by a checking unit.

14. (New) The method of claim 13 further comprising:

generating further test data to check the error detection device by way of data supplied by the error detection device and the addresses of the data.

15. (New) The method of claim 13, wherein the checking unit produces comparative test data from data and addresses which are compared with at least test data of the error detection device or with test data of a memory connected to the error detection device.

16. (New) The method of claim 13, wherein separate bus lines are used for the transmission of data, test data, and addresses between the error detection device and an application memory.

17. (New) An electronic circuit arrangement, for the detection and/or correction of memory access errors in a processor system, the electronic circuit arrangement comprising:

an error detection device;

a processor core connected to the error correction device; and

a memory connected to the error detection device, wherein the error detection device includes a test data generator which generates test data for data to be stored in the memory by way of the data and addresses of the data.

18. (New) The electronic circuit arrangement of claim 17, wherein the error detection device is connected to the memory by way of one or more bus lines.

19. (New) The electronic circuit arrangement of claim 18, wherein separate bus lines are respectively provided for data, test data, and addresses.

20. (New) The electronic circuit arrangement of claim 17, wherein a checking unit is associated with the error detection device.